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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/750,523	SO ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 8/15/07.
- 2a) This action is FINAL.                  2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 12-44 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 12-44 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date: _____   | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

1. The instant application having Application No. 10/750,523 has a total of 44 claims pending in the application; there are 9 independent claims and 35 dependent claims, all of which are ready for examination by the examiner.

### **REJECTIONS BASED ON PRIOR ART**

#### **Claim Rejections - 35 USC § 102**

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 12-23, 25, 29-34 and 41-43** are rejected under 35 U.S.C. 102(b) as being anticipated by Hinton et al. (US 5,500,948).

4. As per **claims 12, 16 and 18**, Hinton discloses a method/system of improving the performance of address translation in a translation lookaside buffer comprising using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd; and consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer;

virtual to physical memory address translation comprising a buffer that uses a single page frame number field for storing odd/even page frame numbers comprising: a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number

field of said translation lookaside buffer; a first register for mapping an even page frame number to said single page frame number fields; and a second register for mapping an odd page frame number to said single page frame number field

as [“**Mini-TLB (TWB),**” defined as “**A small 3-entry instruction mini TLB (6)**” (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein “**the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value**” (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3) “**TWB**” (mini TLB) (Figure 3, Diagram of TWB) in which “**a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked “0” are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked “1” are for odd-numbered 4KB pages, addresses for which bit 12 is a one**” (Column 6, lines 37-63) wherein for a TWB load, “**one set (even or odd) of the TWB registers is loaded with the logical and physical addresses**” (Column 7, lines 5-14). *Hinton also explains “first and second logical registers in said TWB resulting in a first hit signal with respect to said first logical register or a second hit signal with respect to said second logical register... F. gating to a physical address bus a stored value in one of said first or second physical address registers associated with said selected hit signal... issuing a machine bus fetch, upon a condition that said upper order bits of said logical address do not equal a stored value in said first or second logical register in said TWB;... M storing in said TWB said logical address and said second physical*

*address upon a condition that said lower order bits are identical” (Col. 7, line 54-Col. 8; line 45).* Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer). Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field”.

For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, “writing and reading even and odd page frame numbers into a single page frame number field” of a translation lookaside buffer, as claimed by Applicant].

5. As per claims 13, 22, 30, 33 and 42, Hinton discloses The method of claim 12 wherein said bit corresponds to the least significant bit of said virtual page number [Hinton discloses this limitation as “A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page” and explains that “bit 12 selects which of the two entries in the TWB (62) are to be used for this address” (Column 6, lines 37-63; Figure 3). Applicant’s Specification defines a least significant bit as “a least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described)” (Page 3, Paragraph 0026) and

Hinton discloses “a logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page... bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB” (Col. 6, lines 38-43) which clearly corresponds to bit 12 (which is defined as the least significant bit of a virtual page number) of a 32-bit logical address, as defined by Applicant]. Furthermore; it is the Examiner’s position that to one of ordinary skill in the art, the position of the “bit obtained from a virtual page number for the purposes of writing and reading even and odd page frame numbers into a single page frame number field” of a translation lookaside buffer is a matter of design choice as it appears that the invention would perform equally well with (the least significant bit or any other bit within a virtual page number selected to serve the same purpose as disclosed by Hinton and claimed by Applicant)].

6. As per claims 14, 20 and 23, Hinton discloses The method of claim 12 wherein said address translation of said translation look aside buffer is performed by way of using control processor instruction set [Hinton discloses instructions are “fetched from memory, instruction queues, (52) for temporary instruction storage between memory and the cache, instruction pre-decode (54) and post-decode logic (58), address translation logic (62), cache tag logic (60), and the necessary IFU control logic” (Column 3, lines 57-62) and explains that wherein memory may be external (Column 3, line 49); therefore, using a control processor instruction set].

7. As per claims 15, 17 and 19, Hinton discloses The method of claim 12 wherein said consolidating even and odd page frame numbers into said single page frame number fields implements a translation lookaside buffer of reduced size [With respect to this limitation,

Hinton discloses “Mini-TLB (TWB),” defined as “A small 3-entry instruction mini TLB (6)” (Columns 5-6, lines 62-67 and 1-5). Applicant should note that by using “a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value” (Columns 1-2, lines 64-67) wherein even-number pages will only be written within “physical register 0 - 106” and odd-number pages will only be written within “physical register 1 – 104;” therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size, as claimed (See Figures 3 and 7 and related text)].

8. As per claim 21 (new), Hinton discloses A method of implementing a reduced size translation lookaside buffer comprising:  
obtaining a bit obtained from a virtual page number of a virtual address;  
using said bit to determine which one of two storage registers will be used for:  
a) writing page frame number data from said one of two registers into an indexed entry of a single page frame number field of said translation lookaside buffer, said two storage registers comprising a first storage register used for writing even page frame numbers into said single page frame number field when said bit is a first value and a second storage register used for writing odd page frame numbers into said single page frame number field when said bit is a second value, or b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is a second value, said bit used to reduce size of said translation lookaside buffer by way of

consolidating two page frame number fields of said indexed entry into a single page frame number field [Hinton discloses “the instruction pointer is comprised of logical address bits” (Col. 2, lines 9-10) which corresponds to Applicant’s claimed page number wherein “a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked “0” are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked “1” are for odd-numbered 4KB pages, addresses for which bit 12 is a one” (Column 6, lines 37-63) wherein for a TWB load, “one set (even or odd) of the TWB registers is loaded with the logical and physical addresses” (Column 7, lines 5-14) and Figure 3 and explains “the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register’s hit signals, depending on the value of logical address bit 12 (208)” (Col. 7, lines 25-25) (*which comprises reading from the TWB; which corresponds to Applicant’s claimed TLB*) wherein if the instruction is a TWB miss, “then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded” (Figure 7 and related text) [wherein if the instruction is a TWB miss, “then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded” (Figure 7 and related text) (*which comprises writing into the TWB; which corresponds to Applicant’s claimed TLB*) wherein “registers (106) marked “0” are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked “1” are for odd-numbered 4KB pages, addresses for which bit 12 is a one” (Col. 6, lines 56-59)].

[“the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register’s hit signals, depending on the value of logical address bit 12 (208)” (Col. 7, lines 25-25) (*which comprises reading/retrieving from the TWB; which corresponds to Applicant’s claimed TLB*) wherein “registers (106) marked “0” are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked “1” are for odd-numbered 4KB pages, addresses for which bit 12 is a one” (Col. 6, lines 56-59)] (*which comprises writing into the TWB; which corresponds to Applicant’s claimed TLB*]).

9. *Hinton also explains “first and second logical registers in said TWB resulting in a first hit signal with respect to said first logical register or a second hit signal with respect to said second logical register... F. gating to a physical address bus a stored value in one of said first or second physical address registers associated with said selected hit signal (which comprises reading from on of the registers of TWB, as claimed)... issuing a machine bus fetch, upon a condition that said upper order bits of said logical address do not equal a stored value in said first or second logical register in said TWB;... M storing in said TWB said logical address and said second physical address upon a condition that said lower order bits are identical (which comprises writing into one of the registers TWB, as claimed)” (Col. 7, line 54-Col. 8; line 45).*

Hinton discloses [“Mini-TLB (TWB),” defined as “A small 3-entry instruction mini TLB (6)” (Columns 5-6, lines 62-67 and 1-5) which is of mini/reduced size. Applicant should note that by using “a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value

and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 – 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size or mini-TLB, as claimed (See Figures 3 and 7 and related text)].

For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Applicant].

10. As per claims 25 and 43 (new), Hinton discloses The method of Claim 21 wherein said virtual address comprises 32 bits [Hinton discloses this limitation as "A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB" (Column 6, lines 38-43)].

11. As per **claim 29** (new), Hinton discloses A method of performing a write operation using a translation lookaside buffer comprising:

using a bit of a virtual page number, said virtual page number stored in a data register; assessing whether a value of said bit of a virtual page number is 0 or 1; translating a first page frame number stored in a first register to a page frame number field of an indexed entry of said translation lookaside buffer if said value is 0; and writing a second page frame number stored in a second register to said page frame number field of said indexed entry of said translation lookaside buffer if said value is 1, [Hinton discloses “the instruction pointer is comprised of logical address bits” (Col. 2, lines 9-10) which corresponds to Applicant’s claimed page number wherein “a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked “0” are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked “1” are for odd-numbered 4KB pages, addresses for which bit 12 is a one” (Column 6, lines 37-63) wherein for a TWB load, “one set (even or odd) of the TWB registers is loaded with the logical and physical addresses” (Column 7, lines 5-14) and Figure 3 and explains “the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register’s hit signals, depending on the value of logical address bit 12 (208)” (Col. 7, lines 25-25) (*which comprises reading from the TWB; which corresponds to Applicant’s claimed TLB*) wherein if the instruction is a TWB miss, “then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded” (Figure 7 and related text) (*which comprises writing into the*

*TWB; which corresponds to Applicant's claimed TLB)]*

said indexed entry, comprising a single page frame number field used to reduce the size of said translation lookaside buffer [With respect to this limitation, Hinton discloses “Mini-TLB (TWB),” defined as “A small 3-entry instruction mini TLB (6)” (Columns 5-6, lines 62-67 and 1-5). Applicant should note that by using “a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value” (Columns 1-2, lines 64-67) wherein even-number pages will only be written within “physical register 0 - 106” and odd-number pages will only be written within “physical register 1 – 104;” therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size, as claimed (See Figures 3 and 7 and related text)].

12. As per claim 31 (new), Hinton discloses The method of Claim 29 wherein a control processor is used to verify that said first page frame number and said second page frame number are valid as [“bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB. If these bits mismatch, it is considered a TWB miss, and the physical address from the TWB is considered invalid. If the bits match, it is considered a TWB hit, and the physical address bits 12 through 31 stored in the TWB are driven out to the cache on output cache physical address (83) and/or on output physical address (80) to the physical address bus” (Col. 6, lines 37-63)].

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13. As per claim 32 (new) A method of performing a read operation using a translation lookaside buffer comprising:

using a bit of a virtual page number, said virtual page number stored in virtual page number field of said translation lookaside buffer; assessing whether n value of a bit of a virtual page number is 0 or 1; reading a page frame number stored in a page flame number field of an indexed entry of said translation 10okaside buffer, storing said page frame number into a first register if said value is 0; and storing said page frame number into a second register if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer [**The rationale in the rejection to claim 29 is herein incorporated**].

14. As per claim 34 (new) A method of probing for a particular virtual page number of an entry in a translation lookaside buffer comprising:

using a virtual page number stored in a first register; comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer; generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number; and storing said identifying number into a second register [**“Mini-TLB (TWB),” defined as “A small 3-entry instruction mini TLB (6)” (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein “the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value” (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3)**]

**“TWB” (mini TLB) (Figure 3, Diagram of TWB) in which “a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked “0” are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked “1” are for odd-numbered 4KB pages, addresses for which bit 12 is a one” (Column 6, lines 37-63) wherein for a TWB load, “one set (even or odd) of the TWB registers is loaded with the logical and physical addresses” (Column 7, lines 5-14). Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer). Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field.**

For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, “writing and reading even and odd page frame numbers into a single page frame number field” of a translation lookaside buffer, as claimed by Applicant] [See figure 7 and related text].

15. As per claim 41. (New) A reduced size translation lookaside buffer comprising: a virtual page number field used to store a virtual page number; a page frame number field used to store

an even or an odd page frame number, said even or said odd page frame number indicated by a bit from said virtual page number [**The rationale in the rejection to claim 21 is herein incorporated**].

**Claim Rejections - 35 USC § 103**

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

17. **Claim 24** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al. (US 5,500,948).

18. As per **claims 24**, Hinton discloses “The method of claims 3 and 1” [**See rejection to claims 3 and 1 above**]; however, Hinton does not disclose expressly that wherein said TLB control processor instruction set comprises a MIPS control processor instruction set.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an instruction set which comprises a MIPS (Millions Instructions Per Second) processor instruction set which is a well-known processor type. One of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system component designs.

19. **Claims 26 and 44** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al. (US 5,500,948) in view of Bryg et al. (US 6,430,670).

20. As per **claims 26 and 44**, Hinton discloses The method of claim 25 but does not disclose expressly that “said virtual page number is defined by bits [31:12] of said 32 bit virtual address.”

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to **[define a virtual page number by bits [31:12] or any other bit positions of said 32 bit virtual address]**. Applicant has not disclosed that **[defining a virtual page number within specific bit positions of a virtual address]** provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant’s invention to perform equally well with **[a virtual page number defined as bits 13-31 as taught by Hinton]** because **[positions of a virtual page number bits vary depending on the page size used in the virtual mapping and are system-specific as taught by Bryg (Column 4, lines 9-20)]**.

21. **Claims 27-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al. (US 5,500,948) in view of Riedlinger et al. (US 6,446,187).

22. As per **claims 27-28**, Hinton discloses The method of claim; however, Hinton does not discloses “wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes” or “wherein said page mask size comprises 4 kilobytes.”

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to **[use a page mask of any size, including a page mask that ranges from 4 kilobytes to 16 megabytes or that comprises 4 kilobytes for virtual to physical address mapping, such as the system taught by Hinton]**. Applicant has not disclosed that **[having a virtual address utilize a page mask ranging from 4 kilobytes to 16 megabytes or a page mask of 4 kilobytes]** provides an advantage, is used for a particular purpose, or solves a stated

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problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with [any size of page mask] because [it is well known in art that a page mask is used to select a virtual page size (See Riedlinger, Column 4, lines 14-23)].

23. **Claims 35-38 and 40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Hinton et al. (US 5,500,948).

24. As per **claim 35** (new), AAPA discloses A translation lookaside buffer system comprising: a translation lookaside buffer; [**“TLB 104” (Applicant’s Specification; Figure 1 and related text)**]

a first register used for storing a value that indexes an entry in said translation lookaside buffer, said entry comprising a virtual page number field and a single page frame number field; [**“index 132” (Applicant’s Specification; Figure 1 and related text)**]

a second register used for storing a page size of said entry; [**“page mask 136” (Applicant’s Specification; Figure 1 and related text)**]

a third register used for storing a virtual page number of said entry, said virtual page number comprising a bit; [**“Entry Hi” (Applicant’s Specification; Figure 1 and related text)**]

a fourth register used for storing an even page frame number; [**“entry Lo0” (Applicant’s Specification; Figure 1 and related text)**]

and a fifth register used for storing an odd page frame number, [**“entry Lo1” (Applicant’s Specification; Figure 1 and related text)**].

AAPA does not disclose expressly said bit of said virtual page number used to determine whether said even page frame number or said odd page flame number is to be stored in said page

frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page frame number is to be stored in said fourth register or ~aid odd page frame number is' to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer.

Hinton discloses said bit of said virtual page number used to determine whether said even page frame number or said odd page frame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page frame number is to be stored in said fourth register or ~aid odd page frame number is' to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer as [Hinton discloses “**the instruction pointer is comprised of logical address bits**” (Col. 2, lines 9-10) which corresponds to Applicant’s claimed page number wherein “**a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked “0” are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked “1” are for odd-numbered 4KB pages, addresses for which bit 12 is a one**” (Column 6, lines 37-63) wherein for a TWB load, “**one set (even or odd) of the TWB registers is loaded with the logical and physical addresses**” (Column 7, lines 5-14) and Figure 3 and explains “**the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register’s hit signals,**

**depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25) (which comprises reading from the TWB; which corresponds to Applicant's claimed TLB) wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text) (which comprises writing into the TWB; which corresponds to Applicant's claimed TLB) wherein "Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5). Applicant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 – 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size, as claimed (See Figures 3 and 7 and related text)].**

Applicant Admitted Prior Art (AAPA) and Hinton et al. (US 5,500,948) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the TLB system as taught by APPA and further said bit of said virtual page number used to determine whether said even page frame number or said odd page flame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page flame number is to be stored in said

fourth register or said odd page frame number is' to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer as taught by Hinton.

The motivation for doing so would have been because Hinton discloses [**“it is an object of the present invention to provide an address translation mechanism that will translate a logical address from a program counter to a physical address to be used to check an on-chip cache for an instruction” (Col. 1, lines 57-60) for efficient address translation**].

Therefore, it would have been obvious to combine Applicant Admitted Prior Art (AAPA) with Hinton et al. (US 5,500,948) for the benefit of creating a translation lookaside buffer to obtain the invention as specified in claims 35.

25. As per **claim 36** (new), the combination of AAPA and Hinton discloses The method of Claim 35 wherein said read and write operations are performed by way of using a translation lookaside buffer (TLB) control processor instruction set [**Hinton discloses instructions are “fetched from memory, instruction queues, (52) for temporary instruction storage between memory and the cache, instruction pre-decode (54) and post-decode logic (58), address translation logic (62), cache tag logic (60), and the necessary IFU control logic” (Column 3, lines 57-62) and explains that wherein memory may be external (Column 3, line 49); therefore, using a control processor instruction set**].

26. As per **claim 37** (new), the combination of AAPA and Hinton discloses The method of claim 35; however, Hinton does not disclose expressly that wherein said TLB control processor instruction set comprises a MIPS control processor instruction set.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an instruction set which comprises a MIPS (Millions Instructions Per Second) processor instruction set which is a well-known processor type. One of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system component designs.

27. As per claim 38 (new), the combination of AAPA and Hinton discloses The method of Claim 35 wherein said virtual page number is defined by a 32 bit virtual address [Hinton discloses this limitation as “A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page” and explains that “bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB” (Column 6, lines 38-43)].

28. As per claims 40 (new), the combination of AAPA and Hinton discloses The method of Claim 38 wherein said bit comprises the least significant bit (lsb) of said virtual page number [Hinton discloses this limitation as “A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page” and explains that “bit 12 selects which of the two entries in the TWB (62) are to be used for this address” (Column 6, lines 37-63; Figure 3). Applicant’s Specification defines a least significant bit as “a least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described)” (Page 3, Paragraph 0026) and Hinton discloses “a logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page... bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB” (Col. 6, lines 38-43) which clearly

**corresponds to bit 12 (which is defined as the least significant bit of a virtual page number) of a 32-bit logical address, as defined by Applicant]. Furthermore; it is the Examiner's position that to one of ordinary skill in the art, the position of the "bit obtained from a virtual page number for the purposes of writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer is a matter of design choice as it appears that the invention would perform equally well with (the least significant bit or any other bit within a virtual page number selected to serve the same purpose as disclosed by Hinton and claimed by Applicant)].**

29. **Claims 39** is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Hinton et al. (US 5,500,948) as applied to claim 38 above, and further in view of Bryg et al. (US 6,430,670).

30. As per **claims 39**, the combination of AAPA and Hinton discloses The method of claim 38 but does not disclose expressly that "said virtual page number is defined by bits [31:12] of said 32 bit virtual address."

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to **[define a virtual page number by bits [31:12] or any other bit positions of said 32 bit virtual address]**. Applicant has not disclosed that **[defining a virtual page number within specific bit positions of a virtual address]** provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with **[a virtual page number defined as bits 13-31 as taught by Hinton]** because **[positions of a virtual page**

**number bits vary depending on the page size used in the virtual mapping and are system-specific as taught by Bryg (Column 4, lines 9-20)].**

**ACKNOWLEDGEMENT OF ISSUES RAISED BY THE APPLICANT**

31. Applicant's arguments filed August 15, 2007 have been fully considered and are not persuasive.
32. As required by MPEP § 707.07(f), a response to these arguments appears below.

**ARGUMENTS CONCERNING PRIOR ART REJECTIONS**

**1<sup>st</sup> POINT OF ARGUMENT:**

33. Regarding Applicant's remark that Hinton's translation write buffer (TWB) does not teach a translation lookaside buffer (TLB) as Hinton's TWB comprises elements that are functionally different from Applicant's claimed invention; the Examiner would like to point out that Hinton discloses the invention as required by the claims [**See rejection to claims above**]. Furthermore, Hinton expressly discloses [**"Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5); therefore, TWB is a TLB of reduced/mini size.**

34. Regarding Applicant's remark that the TWB disclosed by Hinton performs only write operations and not reading and writing as required by the claims; the Examiner disagrees as Hinton discloses [**"the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit**

12 (208)" (Col. 7, lines 25-25) (*which comprises reading from the TWB; which corresponds to Applicant's claimed TLB*) wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text) (*which comprises writing into the TWB; which corresponds to Applicant's claimed TLB*). Hinton also explains "first and second logical registers in said TWB resulting in a first hit signal with respect to said first logical register or a second hit signal with respect to said second logical register... F. gating to a physical address bus a stored value in one of said first or second physical address registers associated with said selected hit signal (*which comprises reading from one of the registers of TWB, as claimed*)... issuing a machine bus fetch, upon a condition that said upper order bits of said logical address do not equal a stored value in said first or second logical register in said TWB;... M storing in said TWB said logical address and said second physical address upon a condition that said lower order bits are identical (*which comprises writing into one of the registers TWB, as claimed*)" (Col. 7, line 54-Col. 8; line 45).

**2<sup>nd</sup> POINT OF ARGUMENT:**

35. Regarding Applicant's argument that Hinton does not disclose storing even and odd page frame numbers into a single page frame number field of said translation lookaside buffer as Hinton discloses two separate registers; this argument has been considered and is not persuasive.

First of all, the Examiner would like to point out that Applicant's Specification describes storing even and odd page frame numbers into a single page frame number field of said translation lookaside buffer as [**Figure 3 is a relational block diagram illustrating an organizational structure of a mini- TLB system 300 in accordance with an embodiment of**

the invention. The mini-TLB system 300 comprises a miniature version of the previously mentioned translation lookaside buffer described in Figure 1 (herein termed a mini-TLB 304) communicating with a number of mini-TLB registers 308 and a control processor 324. In one embodiment, the mini-TLB 304 is configured by way of instructions executed by the control processor 324. For the mini-TLB 304 shown in Figure 3, the index and page mask registers function in the same manner as was described earlier in Figure 1. In addition, virtual addressing is performed using the addressing format described in Figure 2, in which a 32 bit virtual address is used. Of course, it is contemplated that in other embodiments, virtual addressing may be performed using more or less than 32 bits. In the embodiment shown, the entry Hi 312 register of Figure 3 facilitates storage and read out of a virtual page number associated with bits [31:12] of the virtual addressing format discussed previously. Hence, as illustrated in Figure 3, the virtual page number (VPN) may be either read from or written into a VPN field (or section) 316 of the mini-TLB 304. The VPN is associated with a page frame number (PFN) which is similarly either read from or written into a PFN field 320 of the mini-TLB 304 using the registers shown (i.e., entry Lo0 or entry Lo1 registers). In the embodiment illustrated in Figure 3, only one of the entry Lo registers (either entry Lo0 or entry Lo1) is valid for use during a write operation; for example, the contents of a valid entry Lo register is written into the page frame number (PFN) field 320 associated with a specified page table entry of the mini-TLB 304. In one embodiment, the least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described) is used to determine whether the entry Lo0 or an entry Lo1 register contains valid data for writing into the PFN field 320 of the mini-TLB 304. Similar principles may

be applied during a read from the mini-TLB 304. For example, the least significant bit (lsb) of the VPN may be used to determine which register, either entry Lo0 or entry Lo1, will be used to access valid page frame number data utilized by the control processor 324 during a read operation. In a read operation, for example, the least significant bit (lsb) of a virtual page number is used to store data into either the entry Lo0 register or the entry Lo1 register. In this fashion, both even and odd page frame numbers may be stored or recalled from a single page frame number field of the mini-TLB 304" (Applicant's Specification, Paragraph 0026)]. Therefore, Applicant's Specification discloses two registers and reading/writing to only one of these two registers when reading/writing to TLB. Emphasis added on underlined portions.

Hinton discloses this limitation as ["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3) "TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB

**registers in loaded with the logical and physical addresses” (Column 7, lines 5-14). Hinton also explains “first and second logical registers in said TWB resulting in a first hit signal with respect to said first logical register or a second hit signal with respect to said second logical register... F. gating to a physical address bus a stored value in one of said first or second physical address registers associated with said selected hit signal (which comprises reading from on of the registers of TWB, as claimed)... issuing a machine bus fetch, upon a condition that said upper order bits of said logical address do not equal a stored value in said first or second logical register in said TWB;... M storing in said TWB said logical address and said second physical address upon a condition that said lower order bits are identical (which comprises writing into one of the registers TWB, as claimed)” (Col. 7, line 54-Col. 8; line 45).**

**Therefore, even logical and physical address set is read from/written to TWB and odd logical and physical address set are read from/written to TWB. Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field”.**

**For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, “writing and reading even and odd**

page frame numbers into a single page frame number field” of a translation lookaside buffer, as claimed by Applicant].

**3<sup>RD</sup> POINT OF ARGUMENT:**

36. In response to Applicant’s remark that Hinton does not disclose reducing the size of the TLB; the Examiner disagrees and submits that Hinton discloses this limitation as “[**“Mini-TLB (TWB),” defined as “A small 3-entry instruction mini TLB (6)” (Columns 5-6, lines 62-67 and 1-5) which is of mini/reduced size. Applicant should note that by using “a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value” (Columns 1-2, lines 64-67) wherein even-number pages will only be written within “physical register 0 - 106” and odd-number pages will only be written within “physical register 1 – 104;” therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size or mini-TLB, as claimed (See Figures 3 and 7 and related text)].**

**CLOSING COMMENTS**

**Examiner’s Note**

37. Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially

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teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

**Conclusion**

**a. STATUS OF CLAIMS IN THE APPLICATION**

38. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i):

**a(1) CLAIMS NO LONGER UNDER CONSIDERATION**

39. Claims 1-11 have been cancelled as of amendment filed on August 15, 2007.

**a(2) CLAIMS REJECTED IN THE APPLICATION**

40. Per the instant office action, claims 12-44 have received an action on the merits and are subject of a final rejection.

**b. DIRECTION OF FUTURE CORRESPONDENCES**

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

**IMPORTANT NOTE**

42. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Yaima Campos  
Examiner  
Art Unit 2185

October 24, 2007



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